SEMICONDUCTOR MEMORY DEVICE WITH OFFSET-COMPENSATED SENSING SCHEME

ABSTRACT OF THE DISCLOSURE

Disclosed is a semiconductor memory device which includes an offset-compensated amplifier circuit. The offset-compensated amplifier circuit enables a flip-flop sense amplifier to perform a stable sensing operation irrespective of its own offset voltage. A part of the offset-compensated amplifier circuit is located in a first region (for example, a region that includes the flip-flop sense amplifier), and the other thereof is located in a second region (for example, a region where drivers related to the flip-flop sense amplifier are located). With this distributed arrangement structure, an offset-compensated amplifier circuit can be obtained n the semiconductor memory device.